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EXAMINER	
YAO, KWANG BIN	
ART UNIT	**PAPER NUMBER**
2667	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/810,940	BILIC ET AL.	
	Examiner	Art Unit	
	Kwang B. Yao	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/10/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5, 11, 12, 21-29, 31, 37, 38, 47-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaddis et al. (US 5,815,501).

Gaddis et al. discloses a communication system comprising the following features: regarding claim 1, a network interface device (Fig. 1, ATM-ETHERNET PORTAL; and Fig. 3), comprising: receive logic (Fig. 3, RECEIVE FOL 1), which is coupled to receive from a network a sequence of data packets, each packet comprising respective header data (Fig. 5, ATM HEADER); a protocol processor (Fig. 3, ATM CELL PROCESSOR), coupled to read and process the header data (Fig. 5, ATM HEADER) so as to identify a group of the received packets that contain respective fragments of a data frame, the fragments having a fragment order (Fig. 5, SEGMENT #) within the data frame; and host interface logic (Fig. 3, DMA CONTROLLER 26), which is coupled to a host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) accessible by a host processor (Fig. 3, CONTROL MICROPROCESSOR 20), and is controlled by the protocol processor (Fig. 3, ATM CELL PROCESSOR) so as to allocate space for the data frame in the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24), and to reassemble the fragments of the data frame in the fragment order (Fig. 5, SEGMENT #) in the space

allocated in the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24); regarding claim 2, wherein the protocol processor (Fig. 3, ATM CELL PROCESSOR) is arranged to identify the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N) of the packets and to control the host interface logic (Fig. 3, DMA CONTROLLER 26) so as to reassemble the fragments irrespective of (column 10, lines 46-59) whether the sequence in which the packets are received coincides with the fragment order (Fig. 5, SEGMENT #); regarding claim 3, wherein the protocol processor (Fig. 3, ATM CELL PROCESSOR) is arranged to control the host interface logic (Fig. 3, DMA CONTROLLER 26) so as to allocate the space for the data frame responsive to the header data (Fig. 5, ATM HEADER) of the packet received first in the sequence among the packets in the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N), regardless of (column 10, lines 46-59) whether the packet received first in the sequence is first in the fragment order (Fig. 5, SEGMENT #); regarding claim 5, wherein the protocol processor (Fig. 3, ATM CELL PROCESSOR) is arranged to control the host interface logic (Fig. 3, DMA CONTROLLER 26) so as to allocate the space for the data frame responsive to the packet that is received first in the sequence among the packets in the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N) (Fig. 10); regarding claim 11, wherein the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N) of the received packets is one of a plurality of different groups (Fig. 10, FRAME 1, FRAME 2), the packets in the different groups containing the fragments of different, respective data frames, and wherein the protocol processor (Fig. 3, ATM CELL PROCESSOR) is arranged to identify the different groups and to control the host interface logic (Fig. 3, DMA CONTROLLER 26) so as to simultaneously reassemble (column 10, lines 51-59) the fragments of the different data frames in respectively-allocated spaces in the host memory (Fig. 3, DUAL-PORTED SHARED

MEMORY 24); regarding claim 12, wherein the packets are transmitted over the network and received by the receive logic (Fig. 3, RECEIVE FOL 1) in accordance with one or more communication protocols, whereby the header data (Fig. 5, ATM HEADER) in the packets comprise protocol information (Fig. 5, TYPE), and wherein the protocol processor (Fig. 3, ATM CELL PROCESSOR) is arranged to identify the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N) and to control the host interface logic (Fig. 3, DMA CONTROLLER 26) responsive to the protocol information (Fig. 5, TYPE); regarding claim 21, wherein the protocol processor (Fig. 3, ATM CELL PROCESSOR) is arranged to control the host interface logic (Fig. 3, DMA CONTROLLER 26) so as to write the data packets that do not belong to the identified group to the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) substantially without reassembly processing thereof by the network interface device (Fig. 1, ATM-ETHERNET PORTAL; and Fig. 3); regarding claim 22, wherein the host interface logic (Fig. 3, DMA CONTROLLER 26) comprises a direct memory access DMA engine (Fig. 3, DMA CONTROLLER 26), which is arranged to write the fragments to the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) substantially without involvement of the host processor (Fig. 3, CONTROL MICROPROCESSOR 20); regarding claim 23, wherein the host interface logic (Fig. 3, DMA CONTROLLER 26) is coupled to notify the host processor (Fig. 3, CONTROL MICROPROCESSOR 20) that the fragments of the data frame have been reassembled in the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) only after all of the fragments have been reassembled; regarding claim 24, wherein the protocol processor is arranged to determine a total length of the data frame responsive to the header data of at least one of the packets in the group, and to count a quantity of the data in the fragments reassembled

in the data frame, and to determine that all of the fragments have been reassembled by comparing the total length to the quantity of the data reassembled (column 10, lines 13-34); regarding claim 25, wherein the protocol processor is further arranged to control the host interface logic to write a frame header to the allocated space in the host memory, indicating to the host processor a total length of the data frame (column 10, lines 13-34); regarding claim 26, wherein the receive logic (Fig. 3, RECEIVE FOL 1), protocol processor (Fig. 3, ATM CELL PROCESSOR) and host interface logic (Fig. 3, DMA CONTROLLER 26) are contained together in a single integrated circuit chip, which is separate from the host processor (Fig. 3, CONTROL MICROPROCESSOR 20) and host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24); regarding claim 27, a method for interfacing a host processor (Fig. 3, CONTROL MICROPROCESSOR 20) to a network, comprising: receiving a sequence of data packets from the network at a network adapter (Fig. 1, ATM-ETHERNET PORTAL; and Fig. 3), each packet comprising respective header data (Fig. 5, ATM HEADER); processing the header data (Fig. 5, ATM HEADER) in the adapter so as to identify a group of the received packets that contain respective fragments of a data frame, the fragments having a fragment order (Fig. 5, SEGMENT #) within the data frame; allocating space for the data frame in a host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) accessible by the host processor (Fig. 3, CONTROL MICROPROCESSOR 20); writing the fragments of the data frame from the network adapter (Fig. 1, ATM-ETHERNET PORTAL; and Fig. 3) to the space allocated in the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) so that the fragments are reassembled in the space in the fragment order (Fig. 5, SEGMENT #); and notifying the host processor (Fig. 3, CONTROL MICROPROCESSOR 20) when all of the fragments have been reassembled;

regarding claim 28, wherein processing the header data (Fig. 5, ATM HEADER) comprises identifying the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N) of the packets and preparing the fragments for writing to the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) irrespective of (column 10, lines 46-59) whether the sequence in which the packets are received coincides with the fragment order (Fig. 5, SEGMENT #); regarding claim 29, wherein allocating the space (Fig. 10, SHARED MEMORY) comprises allocating the space (Fig. 10, SHARED MEMORY) for the data frame responsive to the header data (Fig. 5, ATM HEADER) of the packet received first in the sequence among the packets in the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N), regardless of (column 10, lines 46-59) whether the packet received first in the sequence is first in the fragment order (Fig. 5, SEGMENT #); regarding claim 31, wherein allocating the space (Fig. 10, SHARED MEMORY) comprises allocating the space (Fig. 10, SHARED MEMORY) for the data frame responsive to the packet that is received first in the sequence among the packets in the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N); regarding claim 37, wherein the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N) of the received packets is one of a plurality of different groups (Fig. 10, FRAME 1, FRAME 2), the packets in the different groups containing the fragments of different, respective data frames, and wherein processing the header data (Fig. 5, ATM HEADER) comprises identifying the different groups so as to simultaneously reassemble (column 10, lines 51-59) the fragments of the different data frames in respectively-allocated spaces in the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24); regarding claim 38, wherein the packets are transmitted over the network and received by the receive logic (Fig. 3, RECEIVE FOL 1) in accordance with one or more communication protocols, whereby the header data (Fig. 5, ATM HEADER) in the packets comprise protocol

information (Fig. 5, TYPE), and wherein processing the header data (Fig. 5, ATM HEADER) comprises identifying the group (Fig. 10, FRAME 1, CELL 1, 2, ..., N) and preparing the fragments for writing responsive to the protocol information (Fig. 5, TYPE); regarding claim 47, writing the data packets that do not belong to the identified group to the host memory (Fig. 3, DUAL-PORTED SHARED MEMORY 24) substantially without reassembly processing thereof by the network adapter (Fig. 1, ATM-ETHERNET PORTAL; and Fig. 3); regarding claim 48, wherein writing the fragments comprises writing the fragments by direct memory access DMA (Fig. 3, DMA CONTROLLER 26), substantially without involvement of the host processor (Fig. 3, CONTROL MICROPROCESSOR 20); regarding claim 49, wherein processing the header data comprises determining a total length of the data frame responsive to the header data of at least one of the packets in the group, and wherein writing the fragments comprises counting a quantity of the data in the fragments reassembled in the data frame, and comprising determining that all of the fragments have been reassembled by comparing the total length to the quantity of the data reassembled (column 10, lines 13-34); regarding claim 50, wherein processing the header data comprises determining a total length of the data frame responsive to the header data of at least one of the packets in the group, and comprising writing a frame header to the allocated space in the host memory, indicating to the host processor a total length of the data frame (column 10, lines 13-34). See column 9, lines 47 to column 13, line 9.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis et al. (US 5,815,501) in view of Cowger et al. (US 6,314,477).

Gaddis et al. discloses the claimed limitations above. Gaddis et al. does not disclose the following features: regarding claim 4, wherein the protocol processor is arranged to control the host interface logic so as to write each of the fragments to a respective location within the allocated space in the host memory responsive to a fragment offset parameter in the header data of each of the packets; regarding claim 30, wherein writing the fragments comprises writing each of the fragments to a respective location within the allocated space in the host memory responsive to a fragment offset parameter in the header data of each of the packets. Cowger et al. discloses a communication system comprising the following features: regarding claim 4, wherein the protocol processor is arranged to control the host interface logic so as to write each of the fragments to a respective location within the allocated space in the host memory responsive to a fragment offset parameter in the header data of each of the packets (column 1, lines 44-55); regarding claim 30, wherein writing the fragments comprises writing each of the fragments to a respective location within the allocated space in the host memory responsive to a fragment offset parameter in the header data of each of the packets (column 1, lines 44-55). It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Gaddis et al., by using the features, as taught by Cowger et al., in order to provide an efficient and a quick system for locating the position in host memory which to place the data in each received frame. See column 1, lines 10-12.

5. Claims 6-8, 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis et al. (US 5,815,501) in view of Sandorfi et al. (US 5,590,122).

Gaddis et al. discloses the claimed limitations above. Gaddis et al. does not disclose the following features: regarding claim 6, wherein the protocol processor is arranged to determine a size of the space to allocate responsive to a frame length indication in the header data of the packet received first in the sequence; regarding claim 7, wherein the frame length indication comprises one or more fields in the header data indicating an exact length of the data frame; regarding claim 8, wherein the frame length indication comprises one or more fields in the header data indicating an upper bound on a length of the data frame; regarding claim 32, wherein allocating the space comprises determining a size of the space to allocate responsive to a frame length indication in the header data of the packet received first in the sequence; regarding claim 33, wherein the frame length indication comprises one or more fields in the header data indicating an exact length of the data frame; regarding claim 34, wherein the frame length indication comprises one or more fields in the header data indicating an upper bound on a length of the data frame. Sandorfi et al. discloses a communication system comprising the following features: regarding claim 6, wherein the protocol processor is arranged to determine a size of the space (Fig. 6B, steps 232-240, column 2, lines 18-37) to allocate responsive to a frame length indication (Fig. 2B, R_CTL 74, column 4, lines 39-43) in the header data of the packet received first in the sequence; regarding claim 7, wherein the frame length indication (Fig. 2B, R_CTL 74, column 4, lines 39-43) comprises one or more fields in the header data indicating an exact length of the data frame; regarding claim 8, wherein the frame length indication (Fig. 2B, R_CTL 74, column 4, lines 39-43) comprises one or more fields in the header data indicating an

upper bound (column 4, line 43) on a length of the data frame; regarding claim 32, wherein allocating the space comprises determining a size of the space (Fig. 6B, steps 232-240, column 2, lines 18-37) to allocate responsive to a frame length indication (Fig. 2B, R_CTL 74, column 4, lines 39-43) in the header data of the packet received first in the sequence; regarding claim 33, wherein the frame length indication (Fig. 2B, R_CTL 74, column 4, lines 39-43) comprises one or more fields in the header data indicating an exact length of the data frame; regarding claim 34, wherein the frame length indication (Fig. 2B, R_CTL 74, column 4, lines 39-43) comprises one or more fields in the header data indicating an upper bound (column 4, line 43) on a length of the data frame. See column 3-15. It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Gaddis et al., by using the features, as taught by Sandorfi et al., in order to provide less processing time for reassembling packets. See column 2, lines 46-50.

6. Claims 9 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis et al. (US 5,815,501) in view of Unekawa (US 5,706,425).

Gaddis et al. discloses the claimed limitations above. Gaddis et al. does not disclose the following features: regarding claim 9, wherein the protocol processor is arranged to monitor a time required to receive all of the packets in the group, and to control the host interface logic so as to release the space allocated for the data frame if the time exceeds a predetermined limit without all of the fragments in the data frame having been reassembled; regarding claim 35, monitoring a time required to receive all of the packets in the group, and releasing the space allocated for the data frame if the time exceeds a predetermined limit without all of the fragments in the data frame having been reassembled. Unekawa discloses a communication system

comprising the following features: regarding claim 9, wherein the protocol processor is arranged to monitor a time required to receive all of the packets in the group, and to control the host interface logic so as to release the space allocated for the data frame if the time exceeds a predetermined limit without all of the fragments in the data frame having been reassembled (column 1, lines 35-39); regarding claim 35, monitoring a time required to receive all of the packets in the group, and releasing the space allocated for the data frame if the time exceeds a predetermined limit without all of the fragments in the data frame having been reassembled (column 1, lines 35-39). It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Gaddis et al., by using the features, as taught by Unekawa, in order to provide an efficient data communication system.

7. Claims 10 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis et al. (US 5,815,501) in view of Unekawa (US 5,706,425) as applied to claims 9 and 35 above, and further in view of Munger et al. (US 6,502,135).

Gaddis et al. and Unekawa disclose the claimed limitations above. Gaddis et al. and Unekawa do not disclose the following features: regarding claim 10, wherein when the time exceeds the predetermined limit without all of the fragments in the data frame having been reassembled, the protocol processor is arranged to return a message over the network to a source of the packets indicating that the data frame was not received; regarding claim 36, when the time exceeds the predetermined limit without all of the fragments in the data frame having been reassembled, returning a message over the network to a source of the packets indicating that the data frame was not received. Munger et al. discloses a communication system comprising the following features: regarding claim 10, wherein when the time exceeds the predetermined limit

without all of the fragments in the data frame having been reassembled, the protocol processor is arranged to return a message over the network to a source of the packets indicating that the data frame was not received (column 15, lines 56-59); regarding claim 36, when the time exceeds the predetermined limit without all of the fragments in the data frame having been reassembled, returning a message over the network to a source of the packets indicating that the data frame was not received (column 15, lines 56-59). It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Gaddis et al. and Unekawa, by using the features, as taught by Munger et al., in order to provide an efficient data communication system.

8. Claims 13-18, 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis et al. (US 5,815,501) in view of Ding et al. (US 5,699,361).

Gaddis et al. discloses the claimed limitations above. Gaddis et al. does not disclose the following features: regarding claim 13, wherein the one or more communication protocols comprise a plurality of different communication protocols, and wherein the protocol processor is arranged to select the group of packets for reassembly depending on which of the communication protocols was used in transmitting the packets; regarding claim 14, wherein the one or more protocols comprise a network layer protocol; regarding claim 15, wherein the network layer protocol comprises an Internet Protocol IP; regarding claim 16, wherein the one or more protocols comprise a transport layer protocol; regarding claim 17, wherein the transport layer protocol comprises a Transport Control Protocol TCP; regarding claim 18, wherein the transport layer protocol comprises a User Datagram Protocol UDP; regarding claim 39, wherein the one or more communication protocols comprise a plurality of different communication protocols, and

wherein identifying the group comprises selecting the group of packets for reassembly depending on which of the communication protocols was used in transmitting the packets; regarding claim 40, wherein the one or more protocols comprise a network layer protocol; regarding claim 41, wherein the network layer protocol comprises an Internet Protocol IP; regarding claim 42, wherein the one or more protocols comprise a transport layer protocol; regarding claim 43, wherein the transport layer protocol comprises a Transport Control Protocol TCP; regarding claim 44, wherein the transport layer protocol comprises a User Datagram Protocol UDP.

Ding et al. discloses a communication system comprising the following features: regarding claim 13, wherein the one or more communication protocols comprise a plurality of different communication protocols, and wherein the protocol processor is arranged to select the group of packets for reassembly (Fig. 5, IP PROCESS 62, column 3, lines 46-64) depending on which of the communication protocols was used in transmitting the packets; regarding claim 14, wherein the one or more protocols comprise a network layer protocol (Internet Protocol IP, column 2, line 26 to column 4, line 55); regarding claim 15, wherein the network layer protocol comprises an Internet Protocol IP (Internet Protocol IP, column 2, line 26 to column 4, line 55); regarding claim 16, wherein the one or more protocols comprise a transport layer protocol (TCP/UDP, column 2, line 26 to column 4, line 55); regarding claim 17, wherein the transport layer protocol comprises a Transport Control Protocol TCP (TCP/UDP, column 2, line 26 to column 4, line 55); regarding claim 18, wherein the transport layer protocol comprises a User Datagram Protocol UDP (TCP/UDP, column 2, line 26 to column 4, line 55); regarding claim 39, wherein the one or more communication protocols comprise a plurality of different communication protocols, and wherein identifying the group comprises selecting the group of

packets for reassembly (Fig. 5, IP PROCESS 62, column 3, lines 46-64) depending on which of the communication protocols was used in transmitting the packets; regarding claim 40, wherein the one or more protocols comprise a network layer protocol (Internet Protocol IP, column 2, line 26 to column 4, line 55); regarding claim 41, wherein the network layer protocol comprises an Internet Protocol IP (Internet Protocol IP, column 2, line 26 to column 4, line 55); regarding claim 42, wherein the one or more protocols comprise a transport layer protocol (TCP/UDP, column 2, line 26 to column 4, line 55); regarding claim 43, wherein the transport layer protocol comprises a Transport Control Protocol TCP (TCP/UDP, column 2, line 26 to column 4, line 55); regarding claim 44, wherein the transport layer protocol comprises a User Datagram Protocol UDP (TCP/UDP, column 2, line 26 to column 4, line 55). It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Gaddis et al., by using the features, as taught by Ding et al., in order to provide an efficient data communication system by taking advantage of the well known protocols for bursty non-interactive communications. See Ding et al., column 4, lines 43-44.

9. Claims 19, 20, 45, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis et al. (US 5,815,501) in view of Derango et al. (US 6,137,796).

Gaddis et al. discloses the claimed limitations above. Gaddis et al. does not disclose the following features: regarding claim 19, wherein the receive logic is coupled to receive the packets over the network from a plurality of different sources, and wherein the protocol processor is arranged to select the group of packets for reassembly dependent on the packets having been received from one or more chosen sources among the plurality of different sources; regarding claim 20, wherein the selected sources are chosen responsive to a level of reliability of

a connection over the network between the chosen sources and the network interface device; regarding claim 45, wherein receiving the sequence of data packets comprises receiving the packets over the network from a plurality of different sources, and wherein processing the header data comprises selecting the group of packets for reassembly dependent on the packets having been received from one or more chosen sources among the plurality of different sources; regarding claim 46, wherein selecting the group of packets comprises choosing the one or more sources responsive to a level of reliability of a connection over the network between the chose sources and the network interface method.

Derango et al. discloses a communication system comprising the following features: regarding claim 19, wherein the receive logic (a comparator) is coupled to receive the packets over the network from a plurality of different sources (the base stations), and wherein the protocol processor is arranged to select the group of packets for reassembly dependent on the packets having been received from one or more chosen sources among the plurality of different sources (column 1, lines 21-36); regarding claim 20, wherein the selected sources are chosen responsive to a level of reliability of a connection over the network (selecting portions of the signal having the best signal quality) between the chosen sources and the network interface device (column 1, lines 21-36); regarding claim 45, wherein receiving (a comparator) the sequence of data packets comprises receiving the packets over the network from a plurality of different sources (the base stations), and wherein processing the header data comprises selecting the group of packets for reassembly dependent on the packets having been received from one or more chosen sources among the plurality of different sources (column 1, lines 21-36); regarding claim 46, wherein selecting the group of packets comprises choosing the one or more sources

responsive to a level of reliability of a connection over the network (selecting portions of the signal having the best signal quality) between the chose sources and the network interface method (column 1, lines 21-36). It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Gaddis et al., by using the features, as taught by Derango et al., in order to provide a better signal reception probability at the signal destination. See Derango et al., column 1, lines 35-37.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Manchester et al. (US 6,822,960) discloses an ATM switch and method.

Hammermeister et al. (US 6,680,938) discloses a method d for cross connecting data.

Sindhu et al. (US 6,493,347) discloses a router for switching data.

Koga et al. (US 6,470,015) discloses a system for preventing wiretap.

Brockhage et al. (US 6,359,887) discloses a transparent circuit emulation.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang B. Yao whose telephone number is 571-272-3182. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER

Kwang B. Yao
January 18, 2005